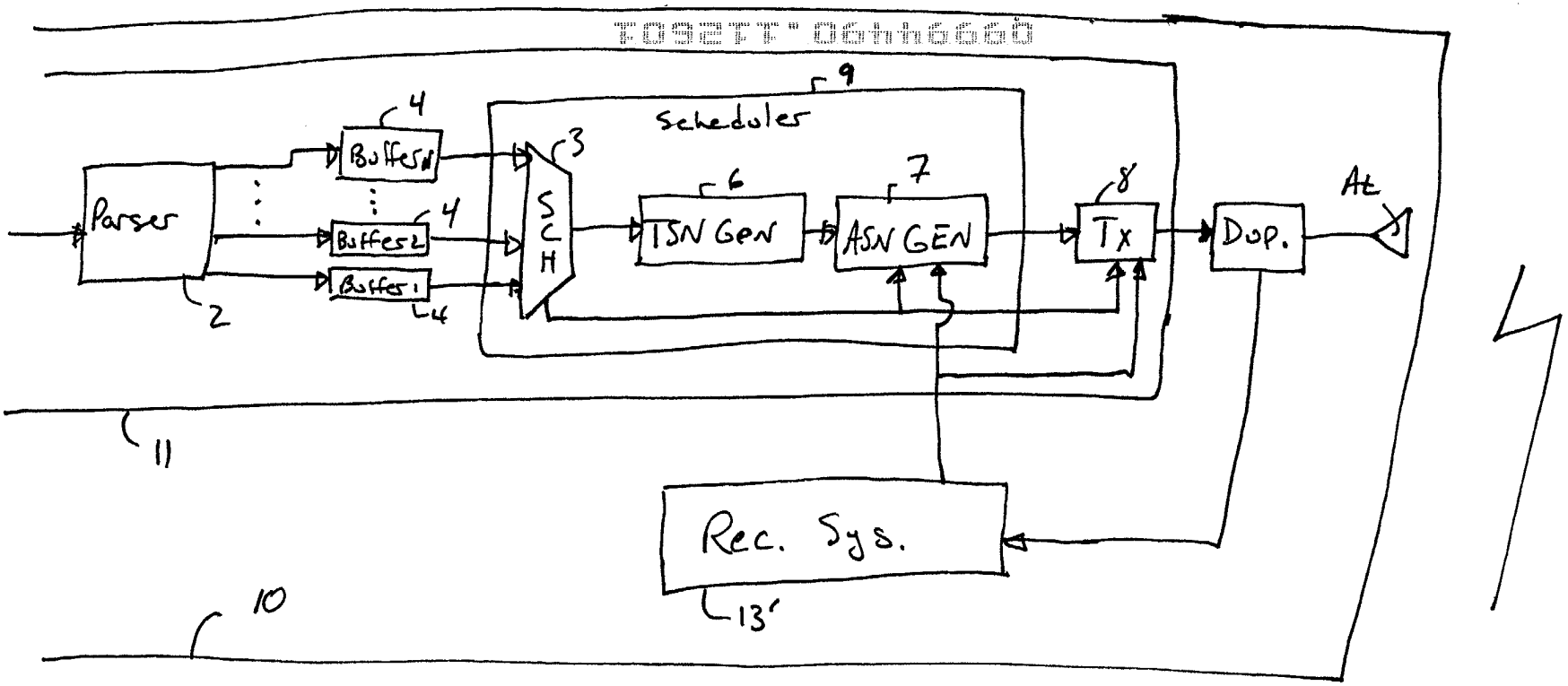
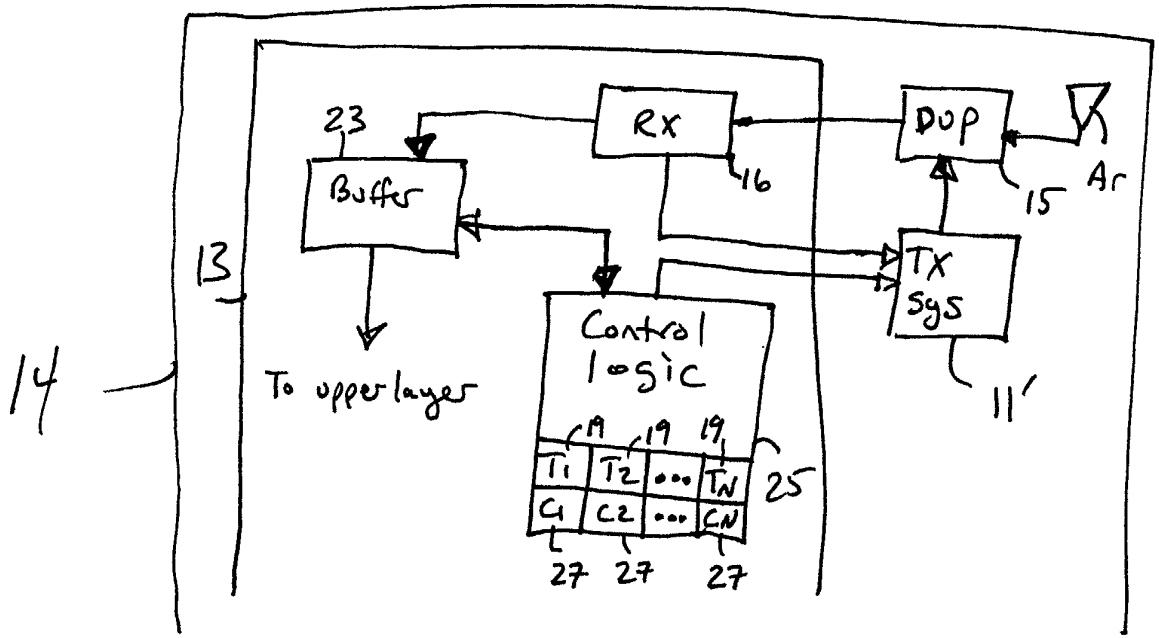

Parser
2
Buffer N
Buffer 2
Buffer 1
4
4
4
SCH
3
Scheduler
9
TSN Gen
6
ASN GEN
7
Tx
8
Dup.
At
11
Rec. Sys.
13'
10

Fig. 1


Rx
16
Dup
15
Ar
23
Buffer
13
TX Sys
11'
Control logic
To upper layer
14
19
19
19
T1
T2
TN
C1
C2
CN
25
27
27
27